

**Communications • Digital Audio • Automotive
Industrial and Medical • Instrumentation • Biometrics**

Einführung

$\mu\text{C} \longleftrightarrow \text{DSP}$

Ausführen von Programmen:

- Steuerungszwecke
(z.B. Aufzugssteuerung)
- Vermittlungstechnik
(Ethernet Switch)
- Datenverarbeitung
- ...

Digitale Signalverarbeitung:

- Digitale Filter
- Codec Implementierung
(Surround Dekodierung &
digital/analog Wandlung)
- Rauschunterdrückung
- Komprimierung
- FFT, MPEG2, HDTV...

Anforderungen an DSP

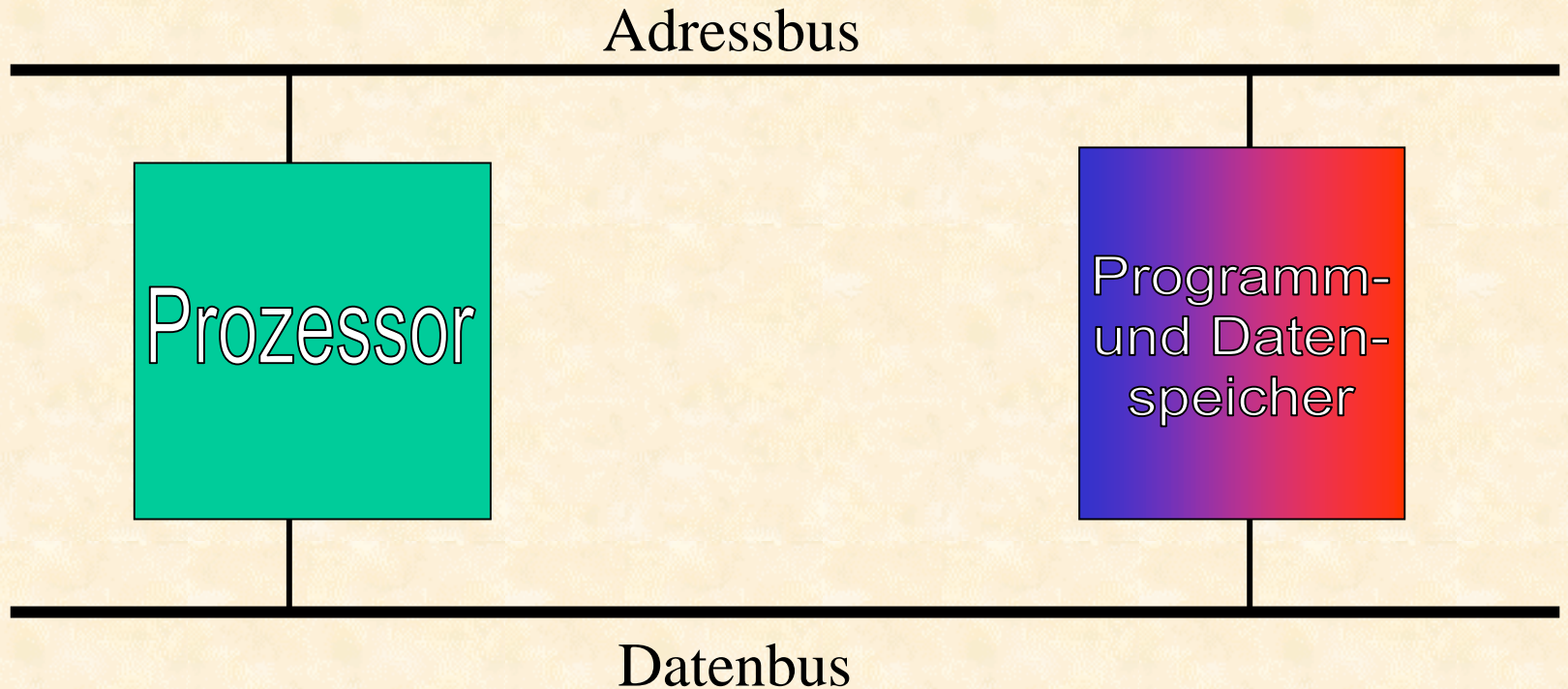
Algorithmen brauchen:

- hohe Datendurchsatzrate
- organisierte Datenströme (Pipelining)
- extrem schnelle Multiplikation / Addition / Subtraktion
- großer Datenspeicher
- hohe Wortbreiten

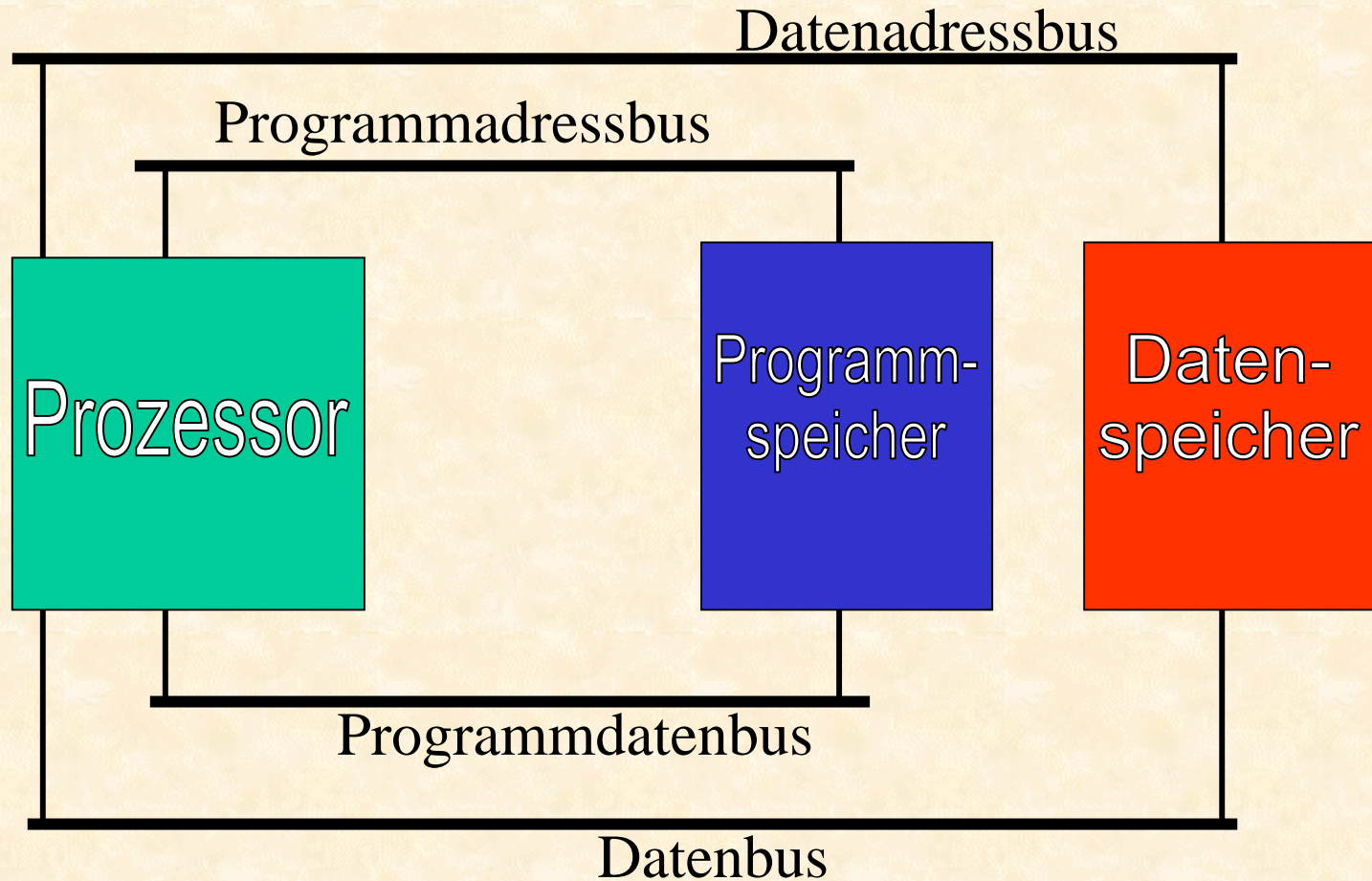
Eigenschaften der SHARC-Familie

- Up to 198 MFLOPS (32-bit floating-point)
- 16K x 32-bit dual-ported on-chip memory
- 64M x 32-bit word external address space
- 2 serial transmit/receive ports support 32-channel TDM
- I2S mode supports up to 8 channels
- Two timers with event capture and PWM
- 12 programmable I/O pins
- 10 DMA channels
- Multiprocessing with two ADSP-21065L SHARC DSPs
- SHARC DSP family binary code compatible
- 3.3 Volt, 208-pin PQFP, 196 ball mBGA
- QFP and BGA packages available

Von Neumann -Architektur

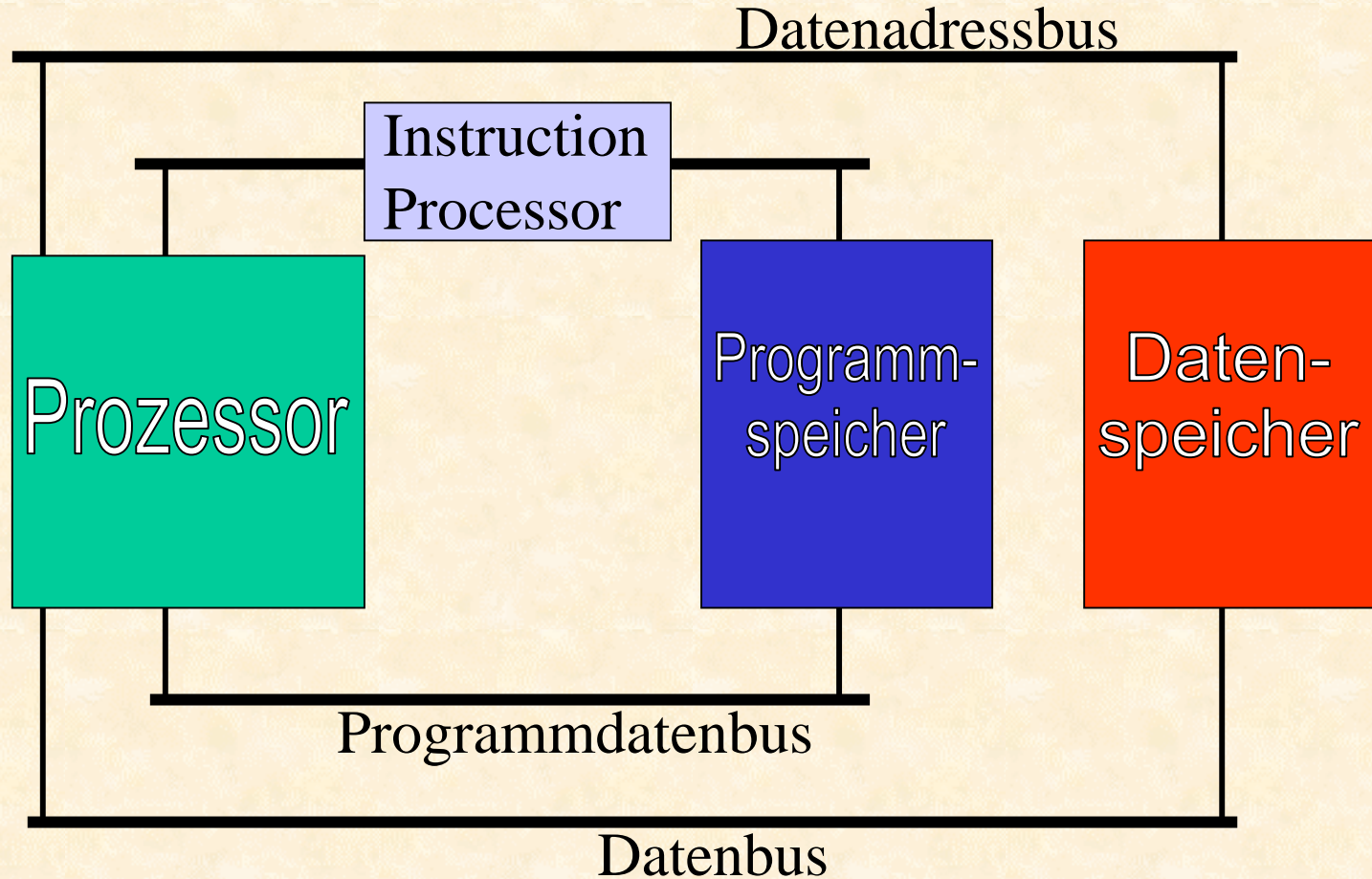


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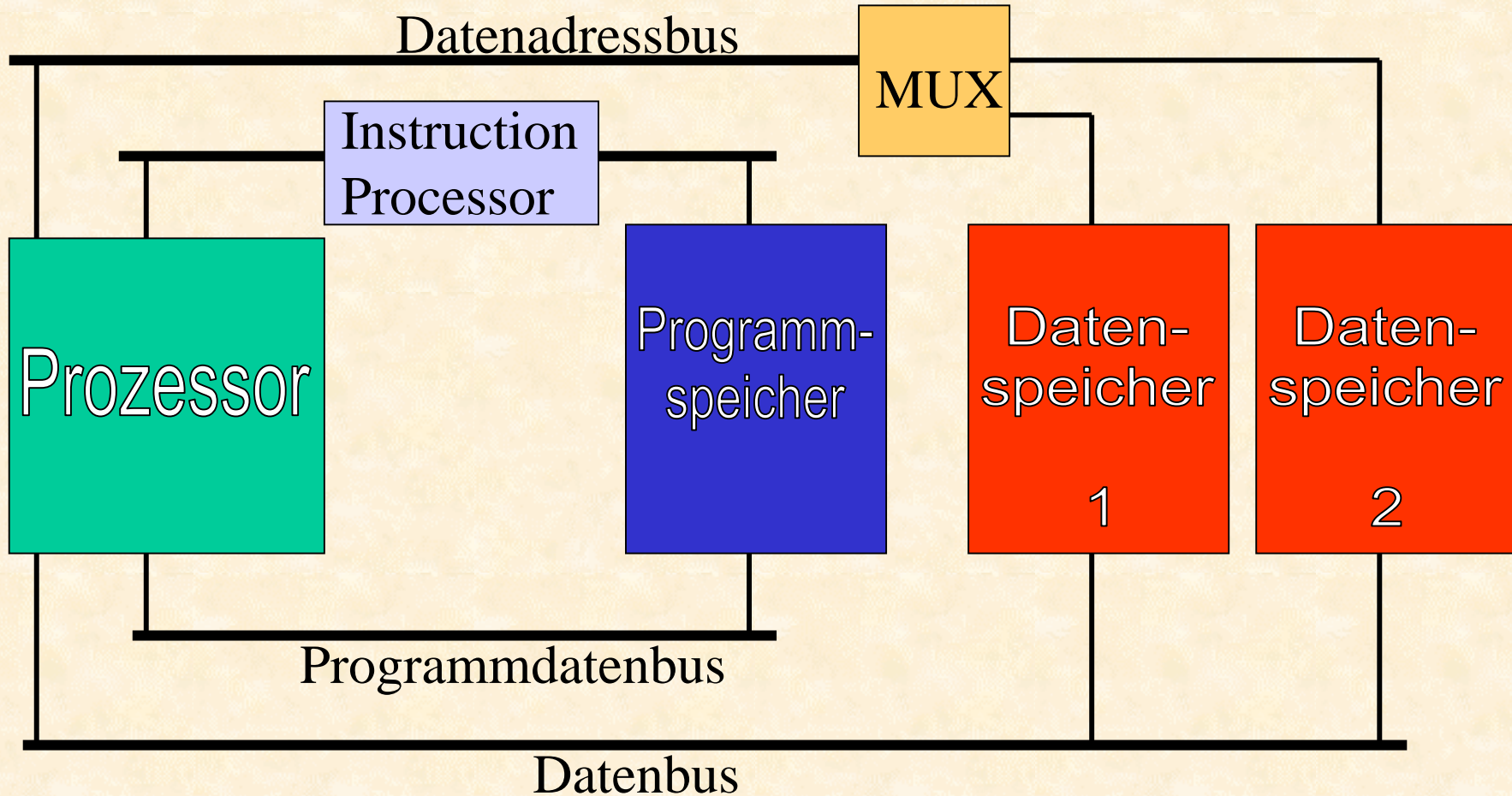
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um IP erweitert

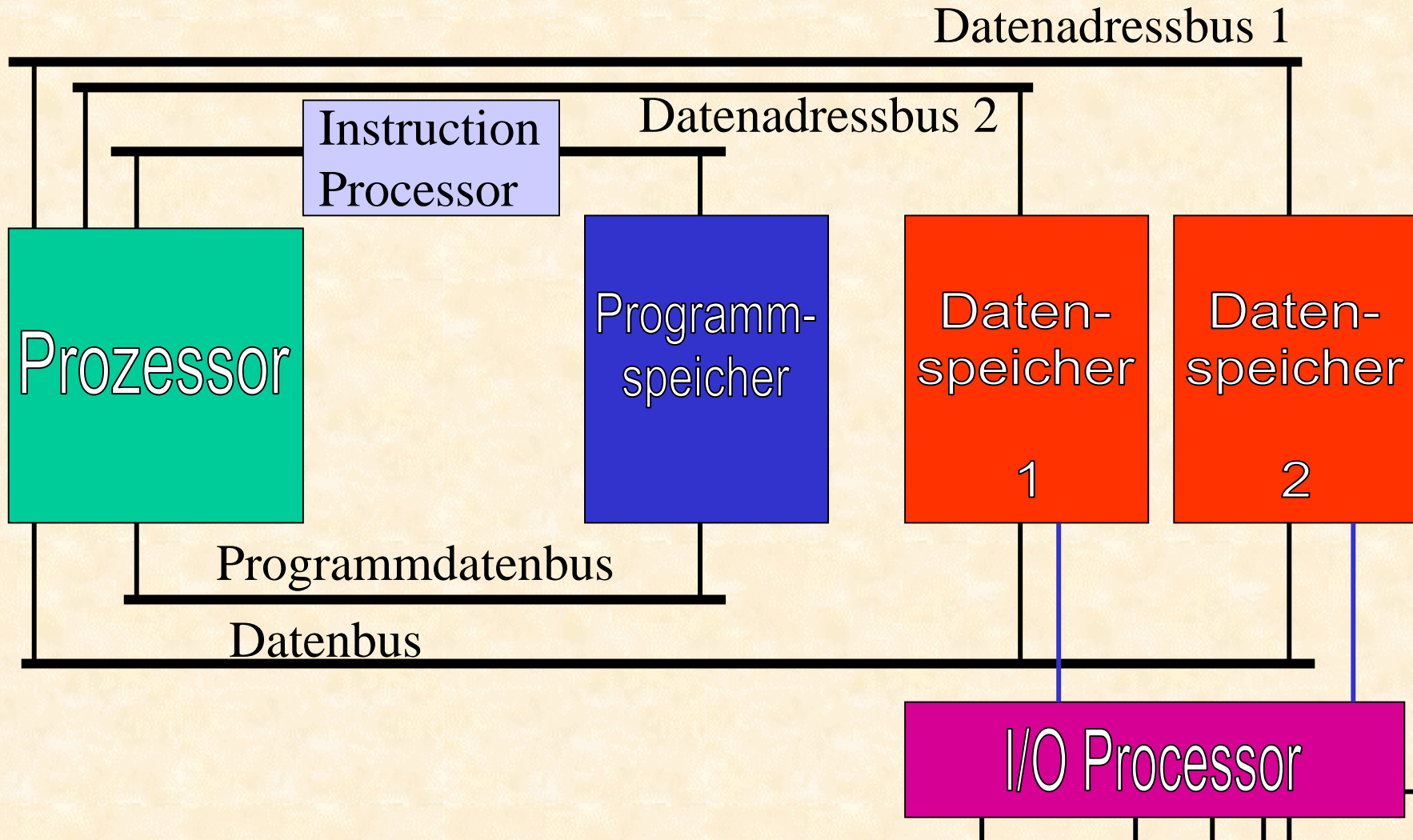


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mit 2 Datenspeichern

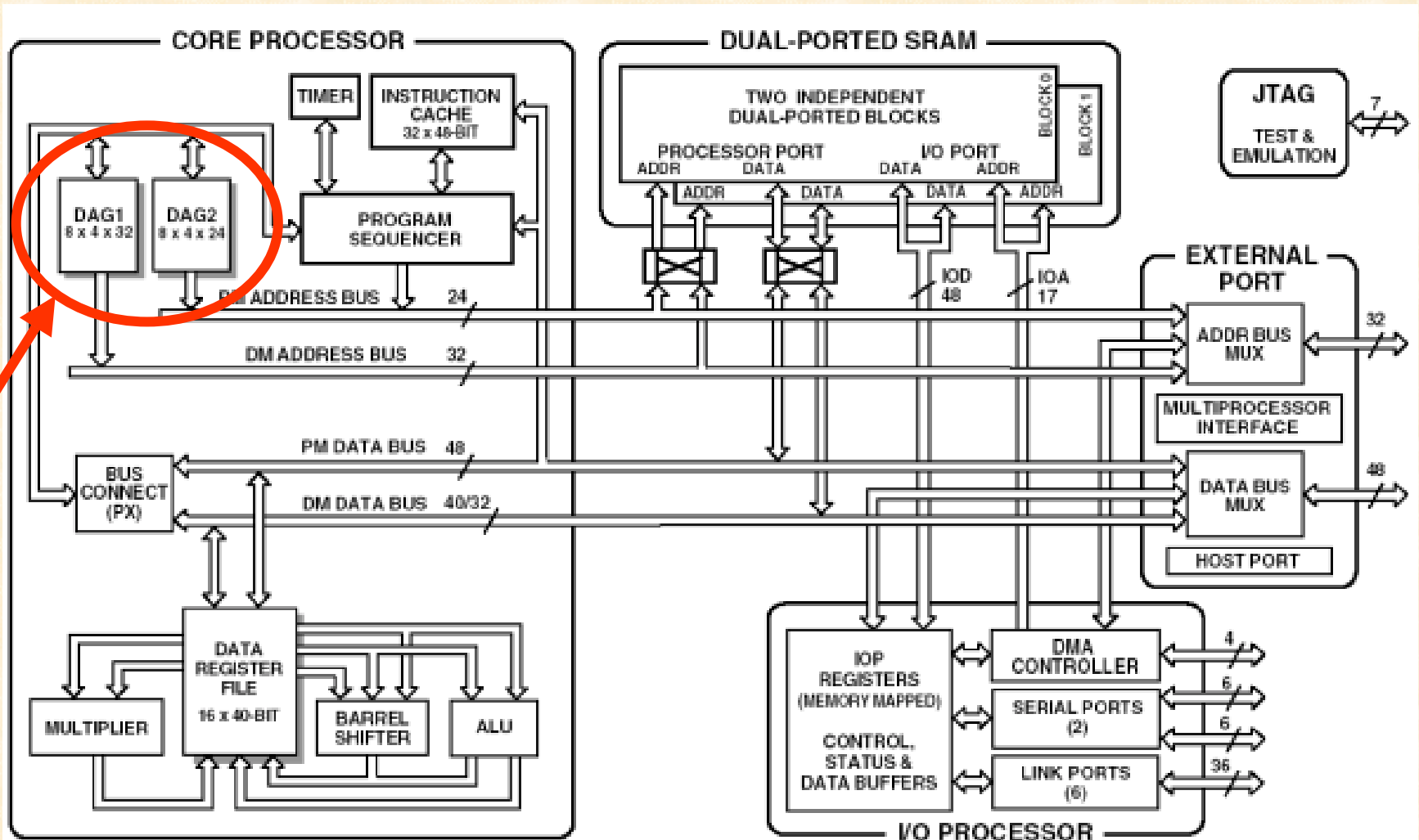


Architektur des SHARC Super Harvard Architektur



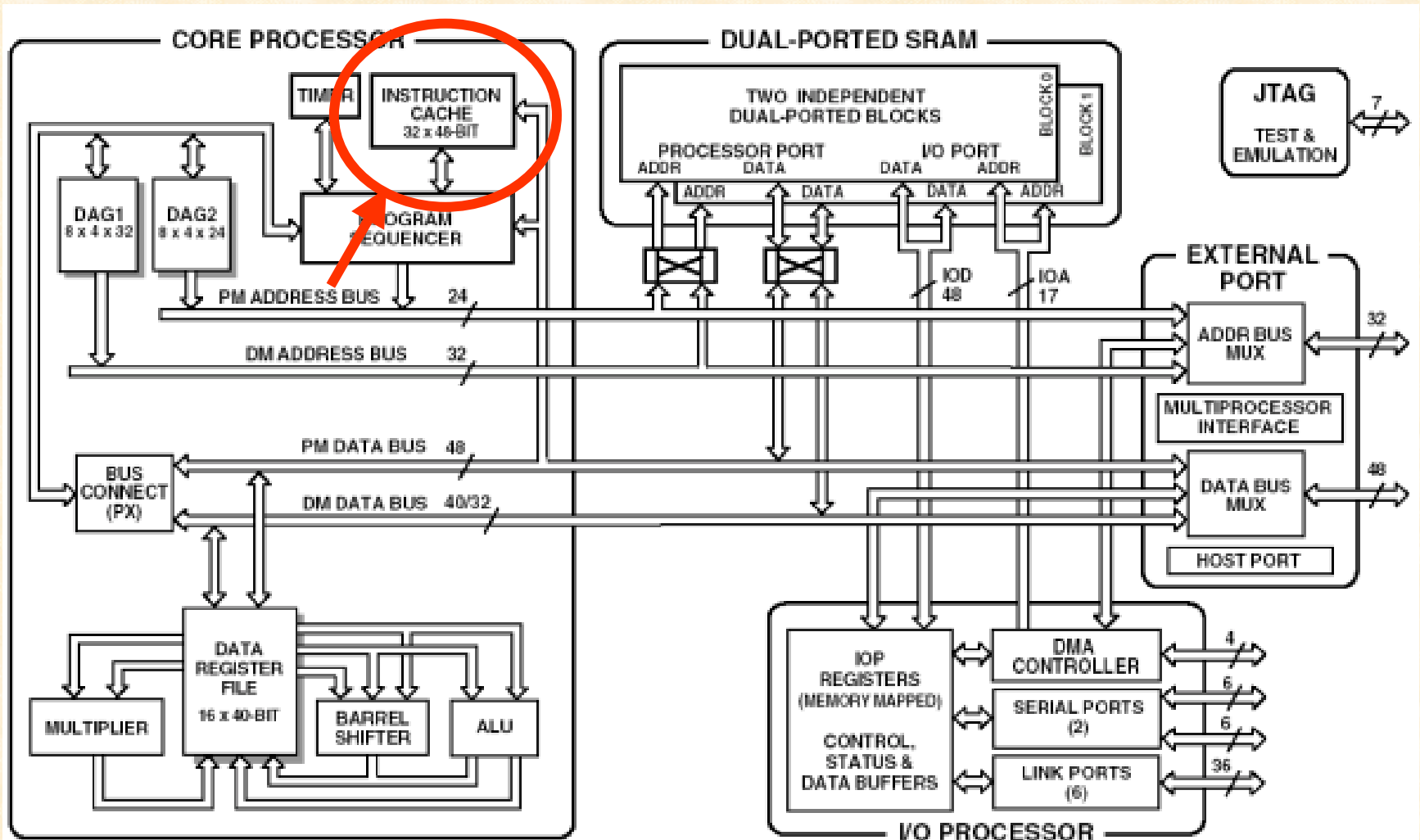
Architektur des SHARC

DAG = Data Adres Generator



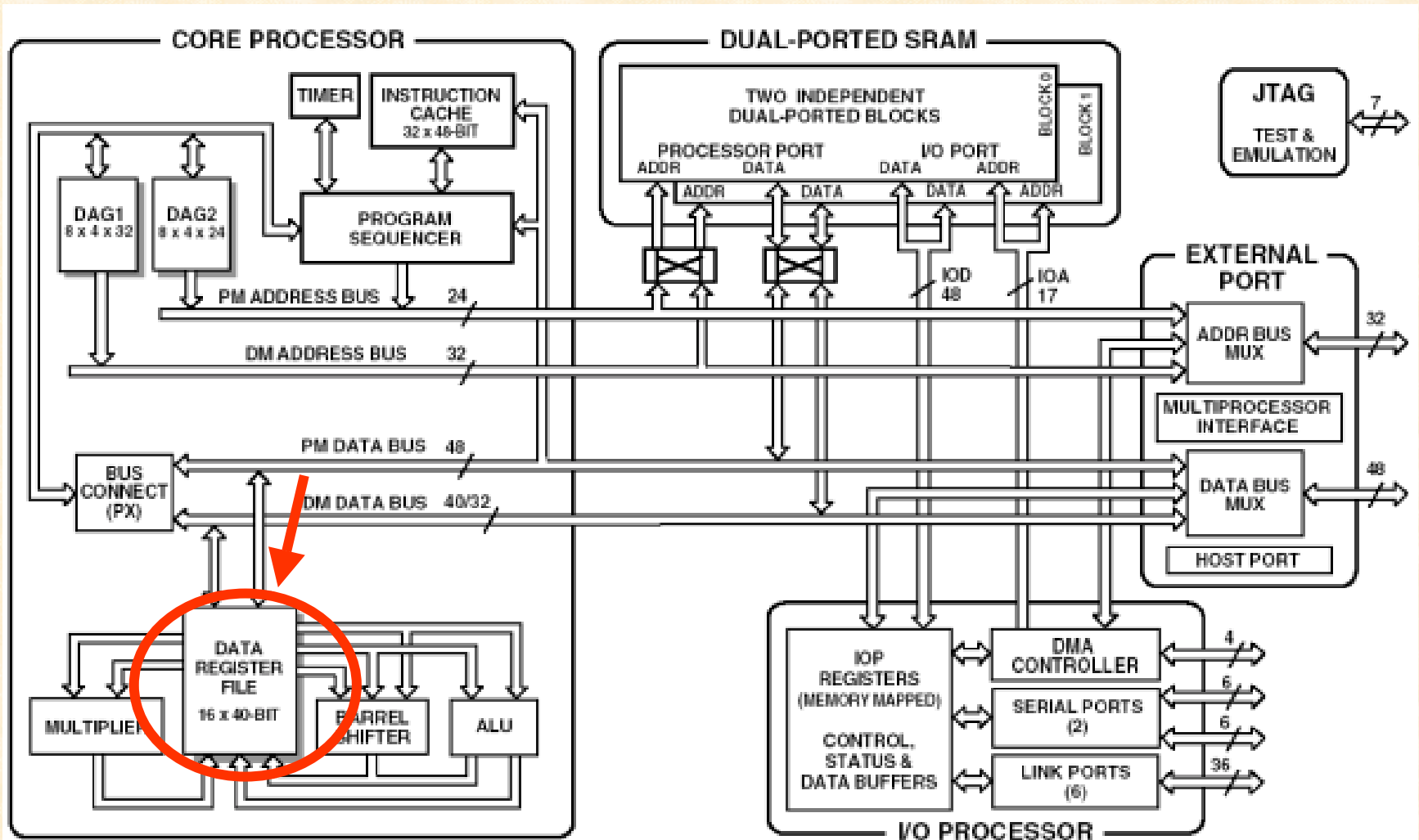
Architektur des SHARC

Instruction Cache

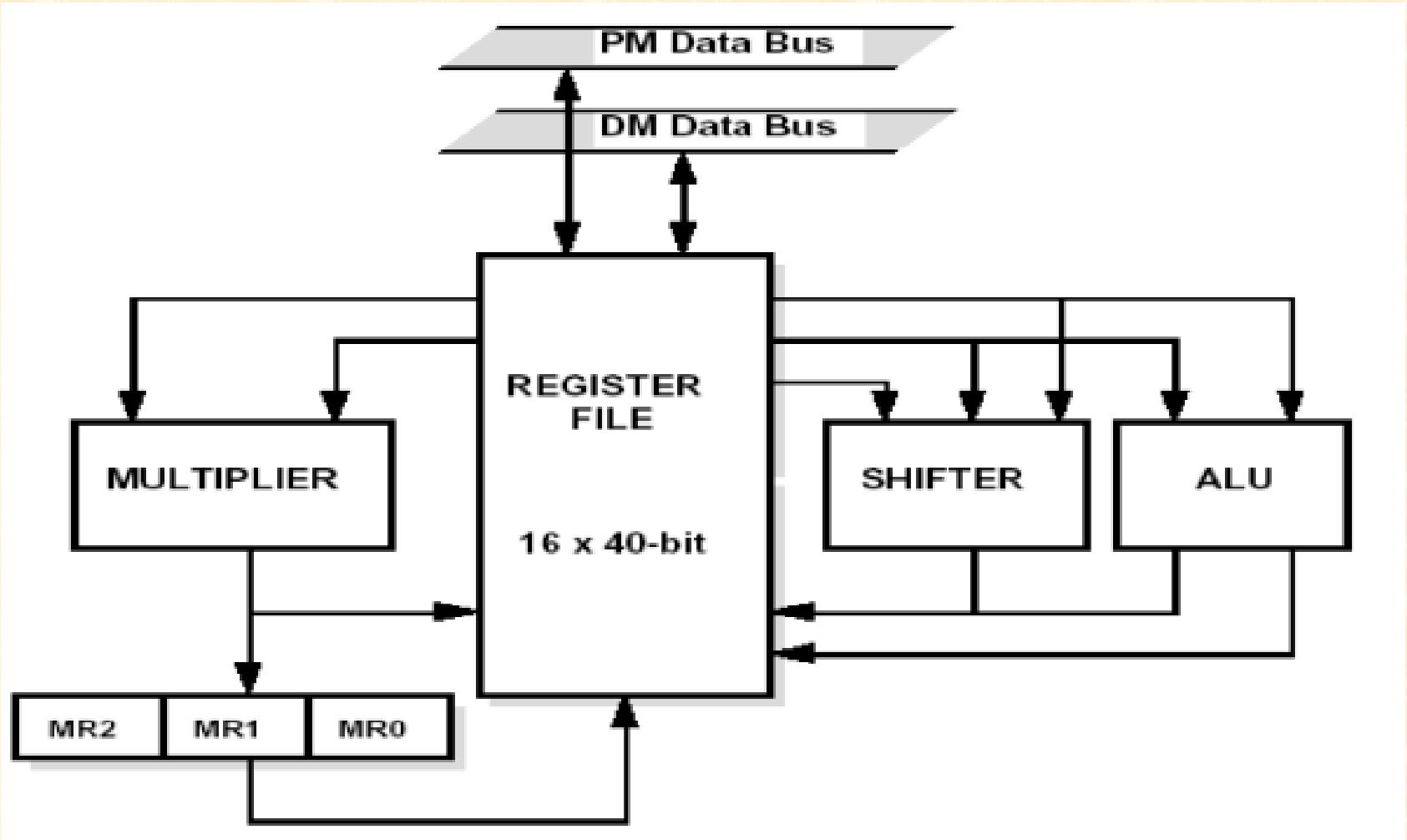


Architektur des SHARC

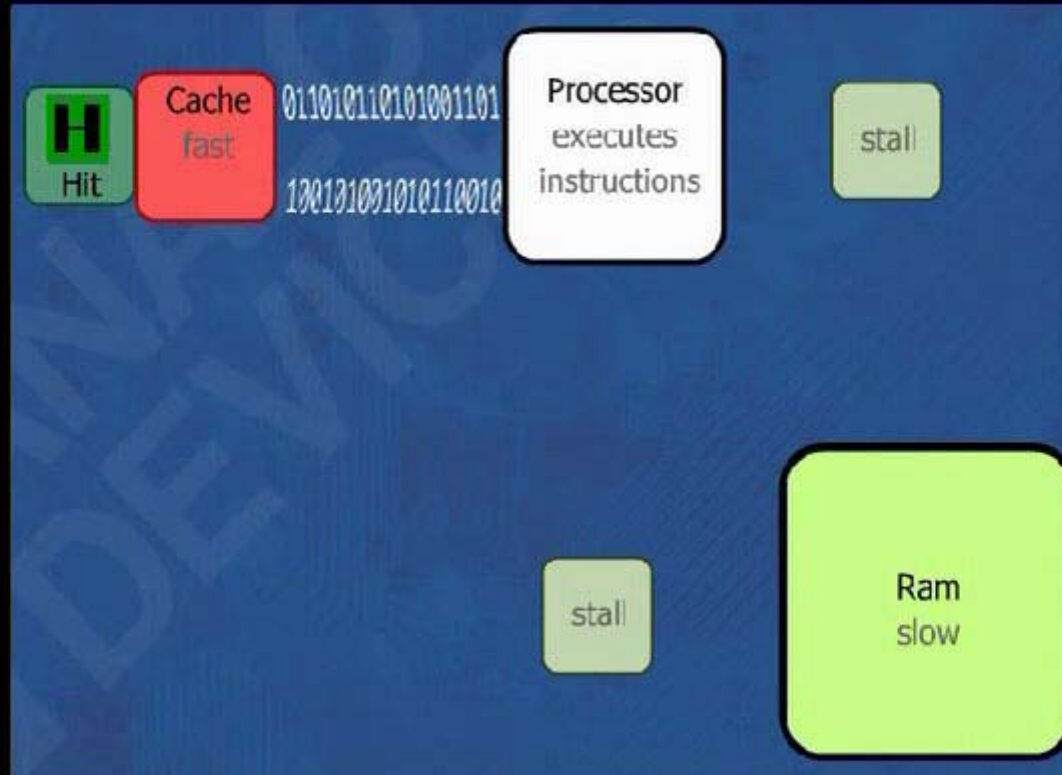
Data Register



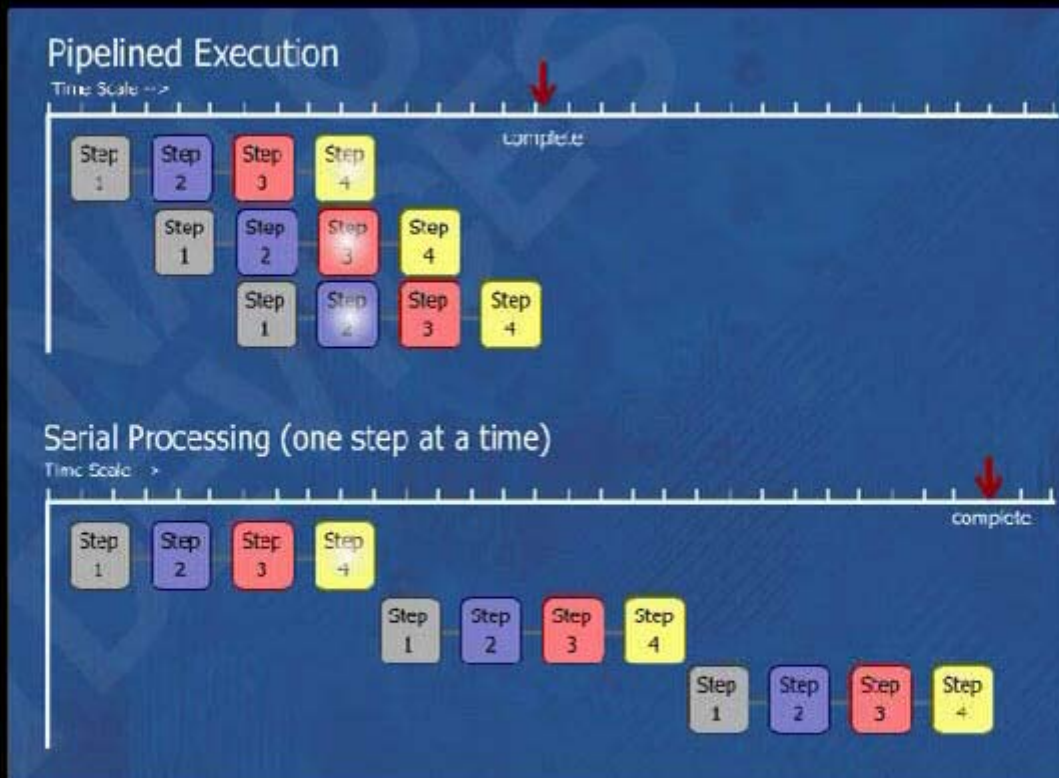
Computation Unit



Pipeline and Cache Overview



Pipelined Execution



Optimierung im Pipeline Viewer

Cycle	Decode	Address	Execute0	Execute1	Execute2	Execute3	Writeback
13	F	A	B	C	D	E	F
14	F	F	A	B	C	D	E
15	LC1 = R7 ; F	F	F	A	B	C	D
16	I0 = R7 ; F	LC1 = R7 ; F	F	F	A	B	C
17	S I0 = R7 ; B	B	LC1 = R7 ; F	F	F	A	B
18	S I0 = R7 ; B	B	B	LC1 = R7 ; F	F	F	A
19	S I0 = R7 ; B	B	B	B	LC1 = R7 ; F	F	A
20	S I0 = R7 ; B	B	B	B	B	LC1 = R7 ; F	A
21	A	A	C	D	E	F	LC1 = R7 ;
22	A	B	C	D	E	F	B
23	F	A	B	C	D	E	C
24	F	F	A	B	C	D	C
25	I0 = R7 ; F	F	F	A	B	C	C
26	I1 = R7 ; F	I0 = R7 ; F	F	F	A	B	C
27	I2 = R7 ; F	I1 = R7 ; F	L0 = R7 ; F	F	F	A	B
28	I3 = R7 ; F	L2 = R7 ; F	L1 = R7 ; F	L0 = R7 ; F	F	F	A
29	P0.H = ... F	L3 = R7 ; F	L2 = R7 ; F	L1 = R7 ; F	I0 = R7 ; F	F	F
30	P0.L = ... F	P0.H = ... F	L3 = R7 ; F	L2 = R7 ; F	I1 = R7 ; F	L0 = R7 ; F	F
31	P0 += 3 ; F	P0.L = ... F	P0.H = ... F	L3 = R7 ; F	I2 = R7 ; F	L1 = R7 ; F	L0 = R7 ; F
32	P1 = 13 ; F	P0 += 8 ; F	P0.L = ... F	P0.H = ... F	I3 = R7 ; F	L2 = R7 ; F	L1 = R7 ; F

Multiprocessing

„Langsame“ Cluster-Anordnung (nur 40 Mbyte/s)

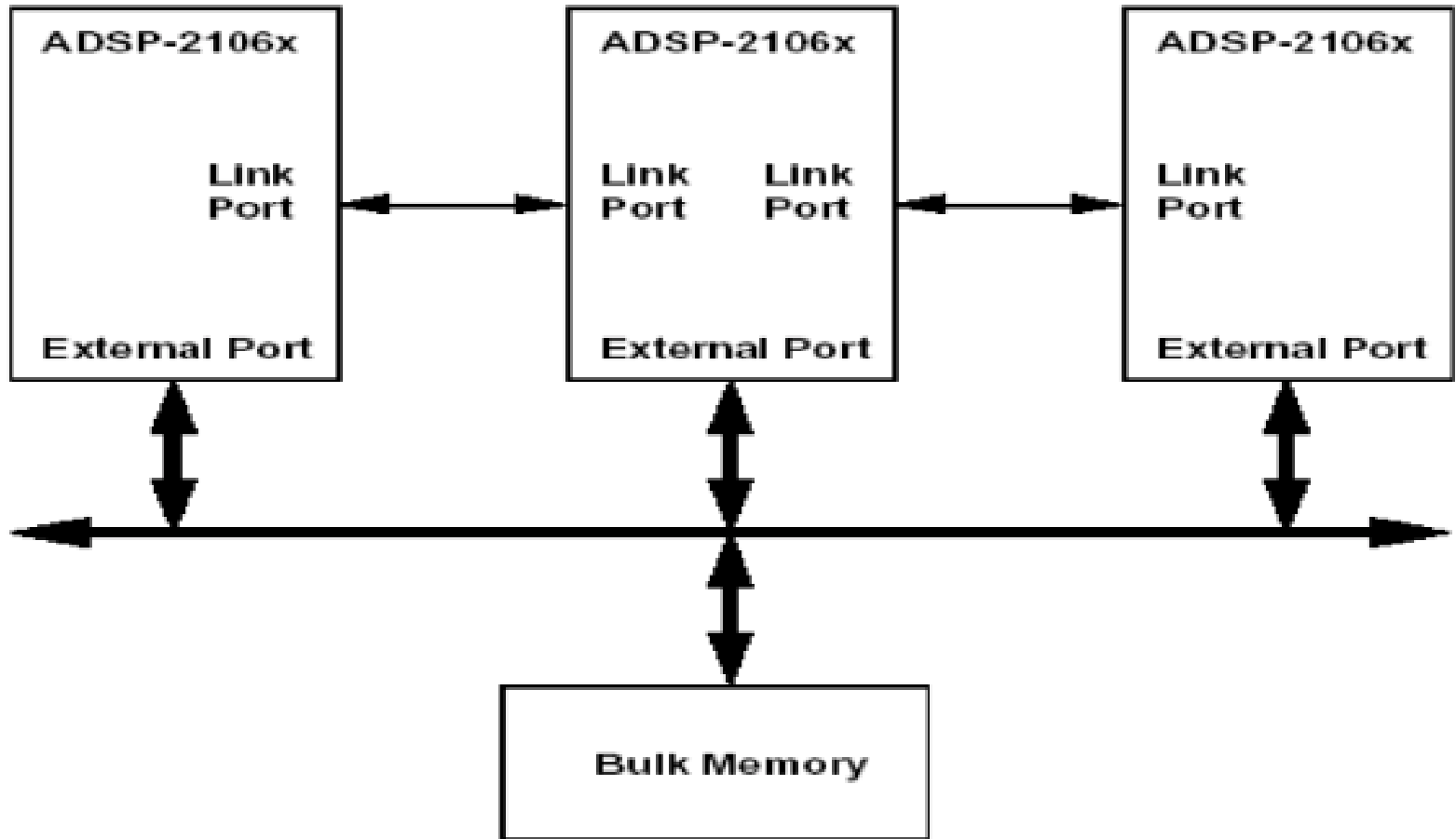
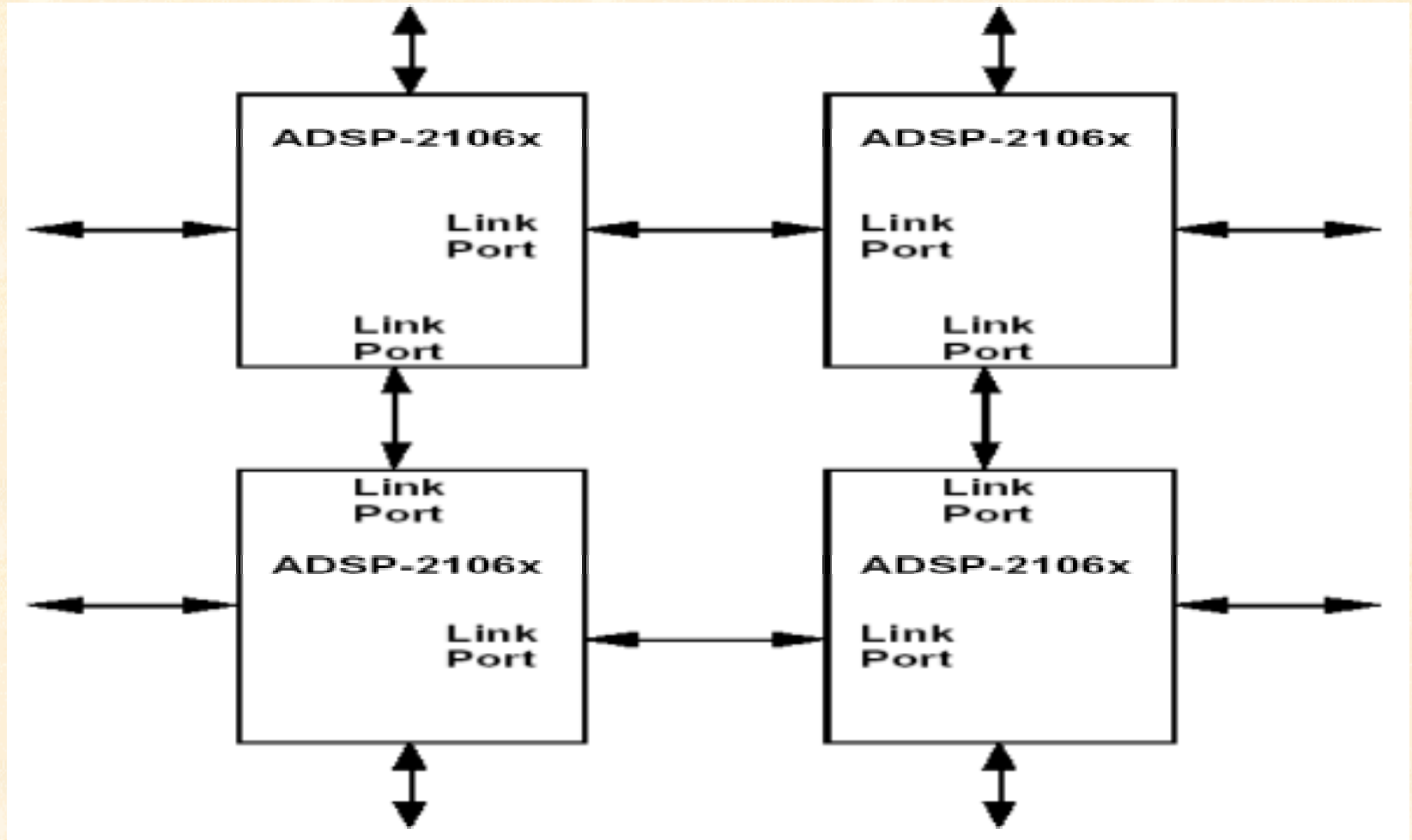


Figure 7.3 Cluster Multiprocessing

Multiprocessing

2D-Mesh-Anordnung (240 Mbyte/s)



Fragen?

Weitere Informationen auch unter:

www.analog.com

www.stonee.de